IN THE DRAWINGS:

By way of a separate letter attached hereto, applicants propose to amend Fig. 3A to change the reference numeral "20" to –10--, and to amend Fig. 4 to change the reference numeral "28" to –29--. In anticipation of the Examiner's approval, the changes have been incorporated into the formal drawings submitted herewith.

#9/Drawg
11-6-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Sitaram YADAVALLI, et al.

Serial No.:	09/531,910	Group Art Unit:	2123
Filed:	March 20, 2000	Examiner:	H. Day

FOR: METHOD AND APPARATUS FOR MODELING AND CIRCUITS WITH ASYNCHRONOUS BEHAVIOR

PROPOSED CHANGES TO THE DRAWINGS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed July 16, 2003, applicants propose to amend Fig. 3A to change the reference numeral "20" to –10--, and to amend Fig. 4 to change the reference numeral "28" to –29--. The changes are marked in red on the attached sheets. In anticipation of the Examiner's approval, the changes have also been incorporated into the formal drawings submitted herewith.

If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

October 17, 2003
Date

Paul E. Steiner
Reg. No. 41,326
(703) 633 - 6830

Intel Americas
LF3
4030 Lafayette Center Drive
Chantilly, VA 20151

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on:

10/23/03
Date of Deposit

Annie Pearson
Name of Person Mailing Correspondence

Annie Pearson 10/23/03
Signature Date

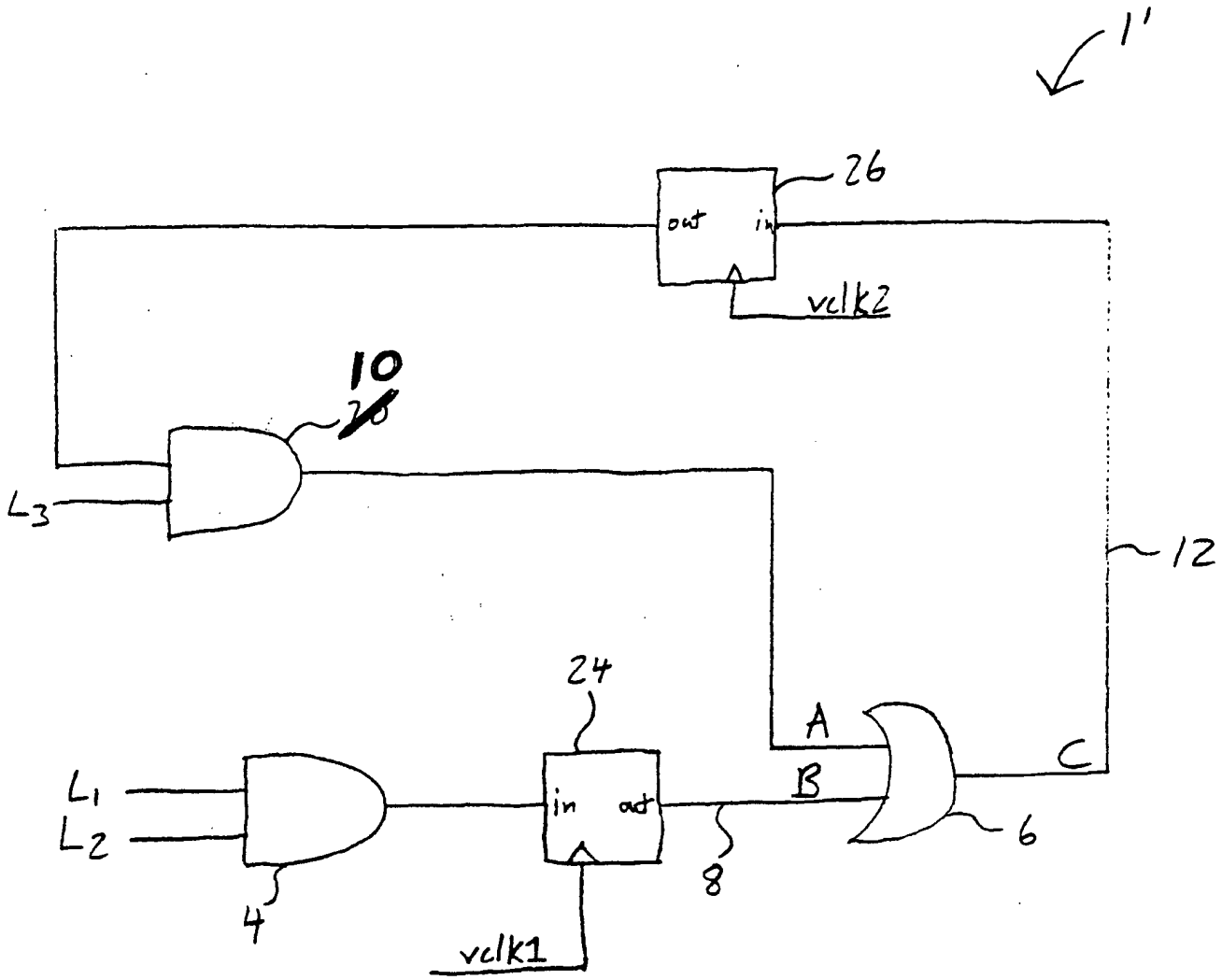


Fig. 3A

Approved.
HD 12/31/03

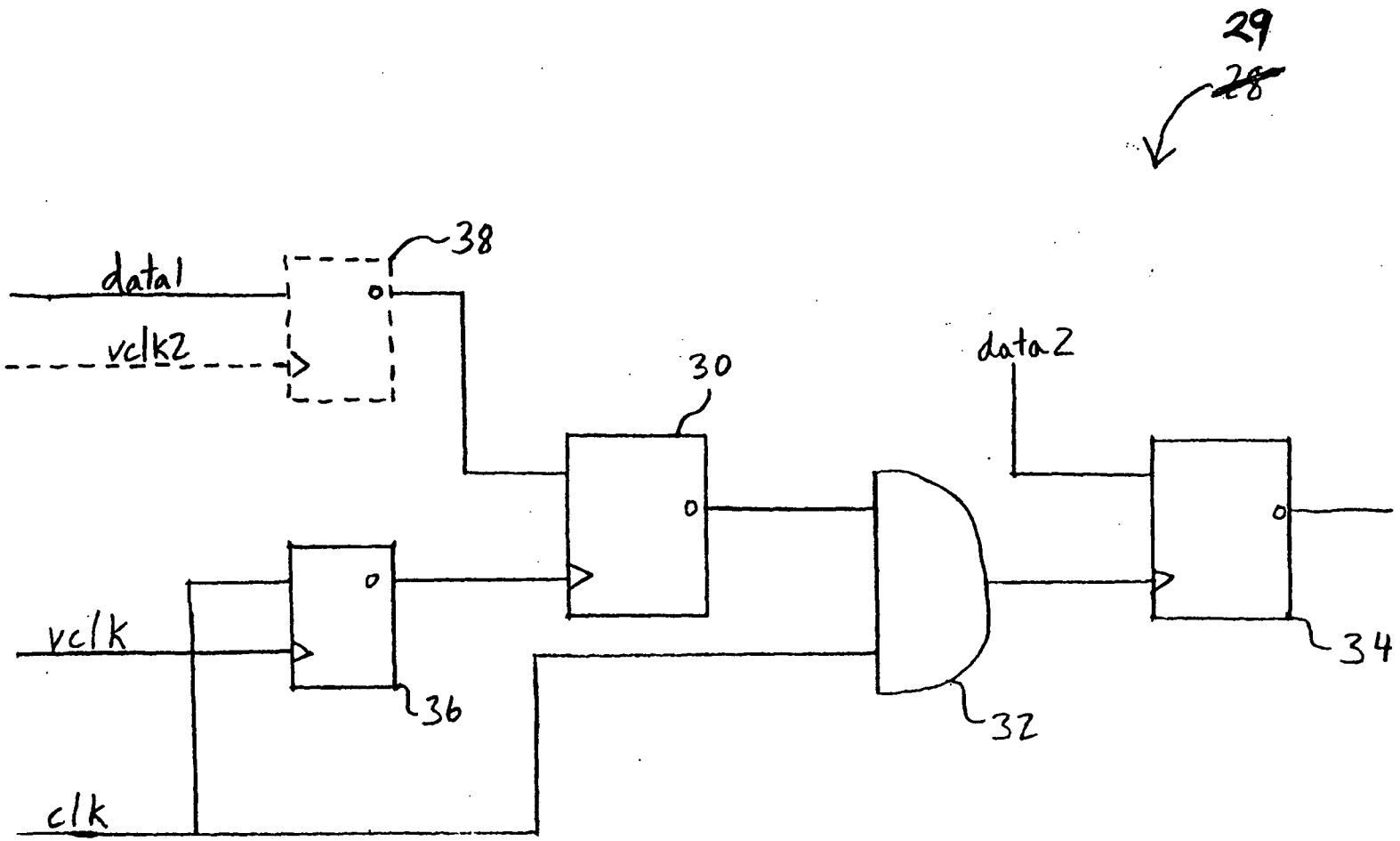
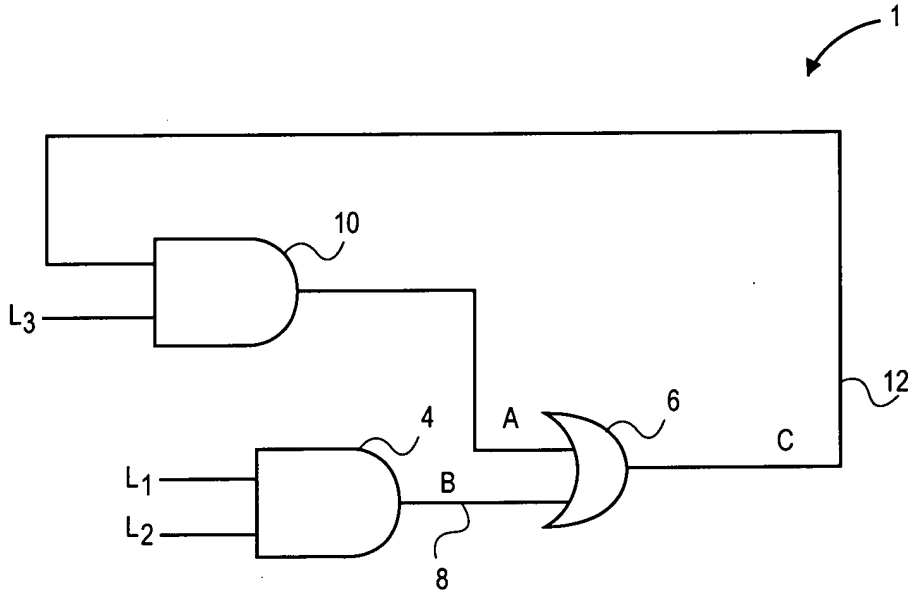


Fig. 4



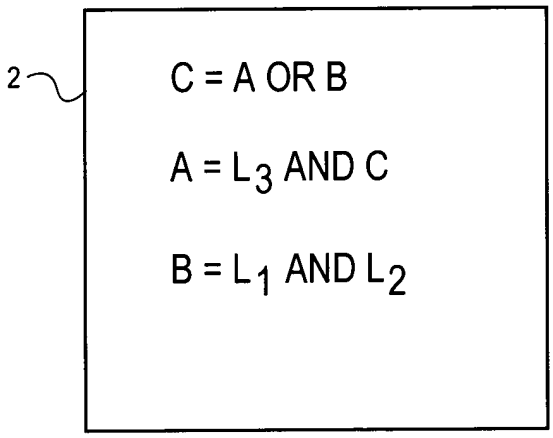


FIG. 1
(PRIOR ART)

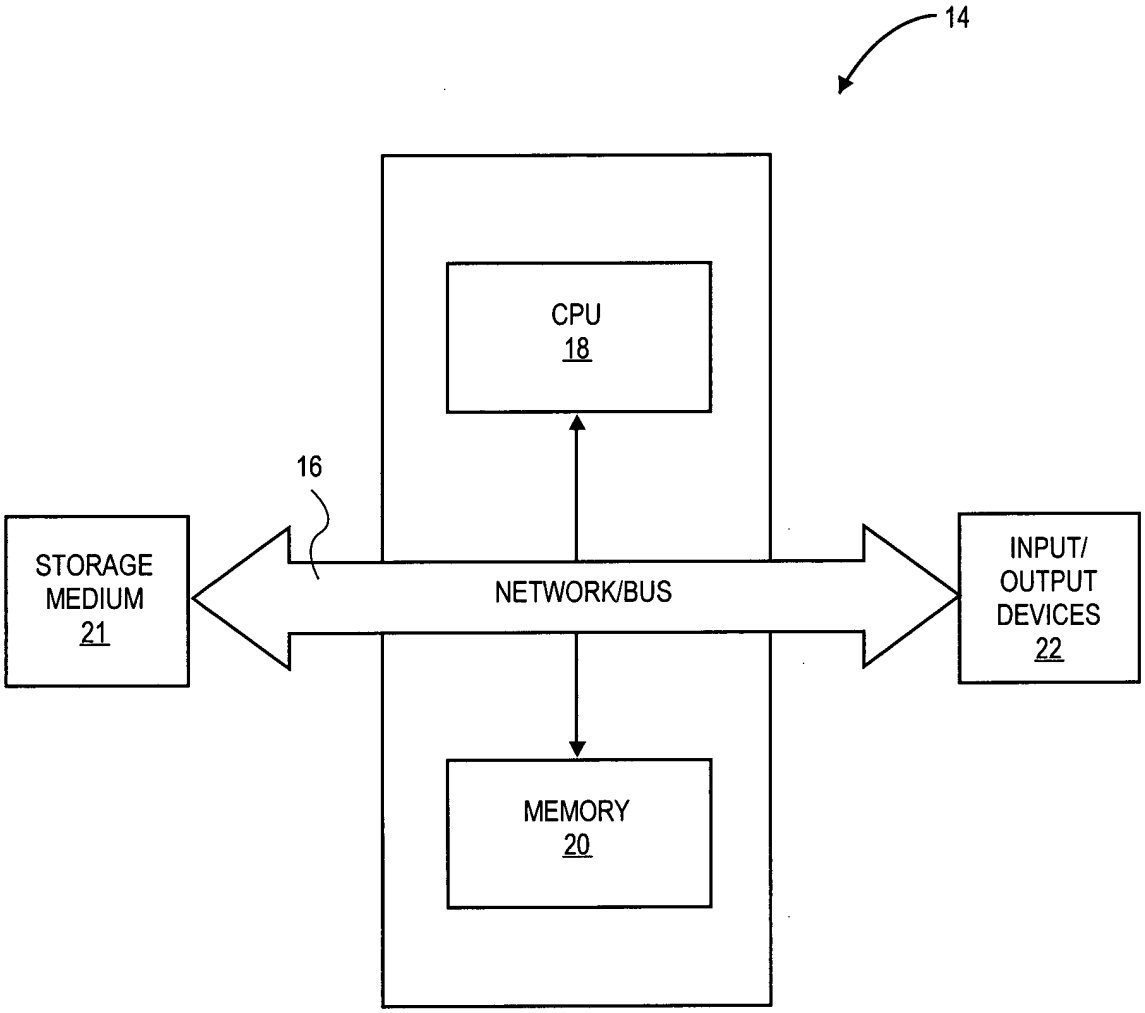


FIG. 2

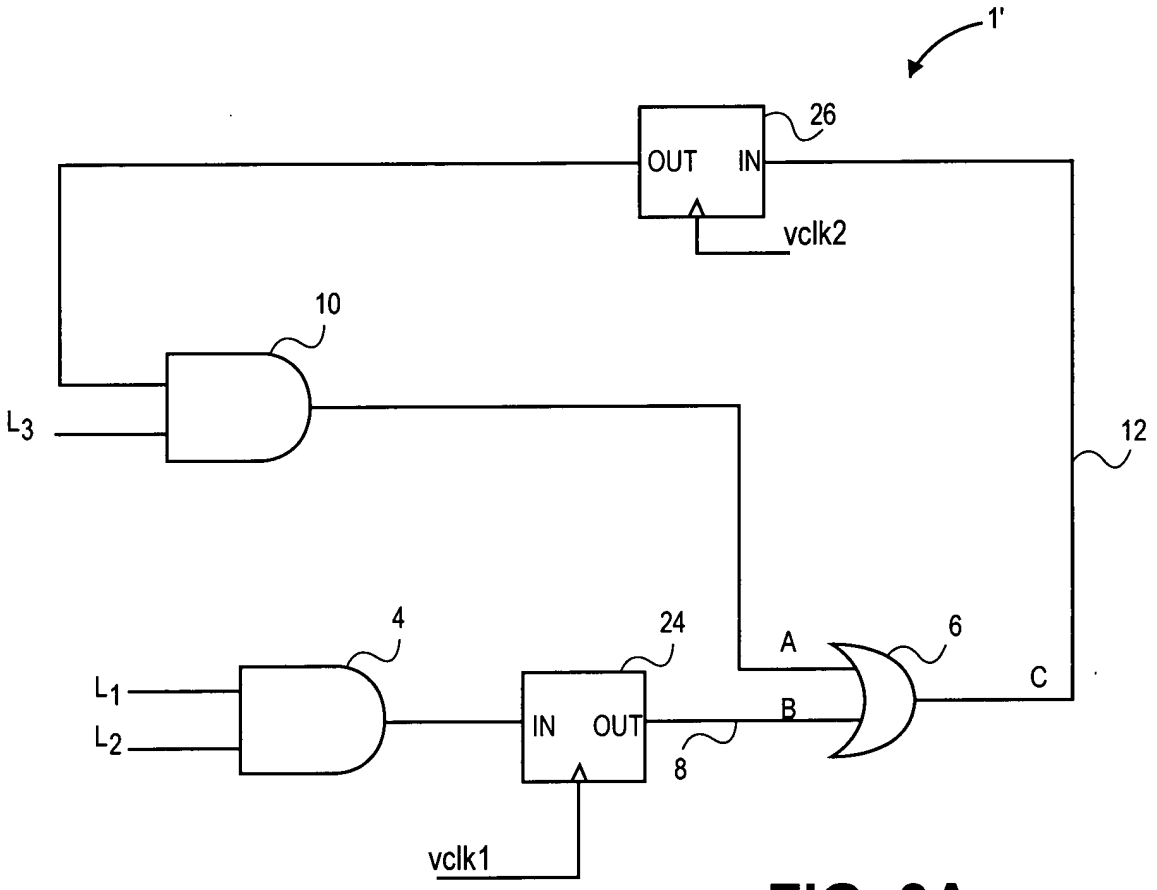


FIG. 3A

```
in24 = L1 and L2
out24 = if (vclk1 == HIGH) then in24//change state
        else out24//retain state
B = out24
C = A or B
in26 = C
out26 = if(vclk2 == high) then in26//change state
        else out26//retain state
A = L3 and out26
```

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```
module fig1 (L1, L2, L3, vclk1, vclk2, .. )
input L1, L2, L3, vclk1, vclk2;

        and     g14 ( in24, L1, L2 );
        vdelement g24 ( out24, vclk1, in24 );
        or      g16 ( in26, A, out24 );
        vdelement g26 ( out26, vclk2, in26 );
        and     g20 ( A, L3, out26 );

endmodule

primitive vdelement (out, vclk, in)
output out;
reg out;
input vclk, in;

table
// vclk  data    out     out_new
  1      1:      ?        :1;
  1      0:      ?        :0;
  0      ?:      ?        :-;// - means 'no change', i.e. retain previous value
endtable
endprimitive
```

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FIG. 3B

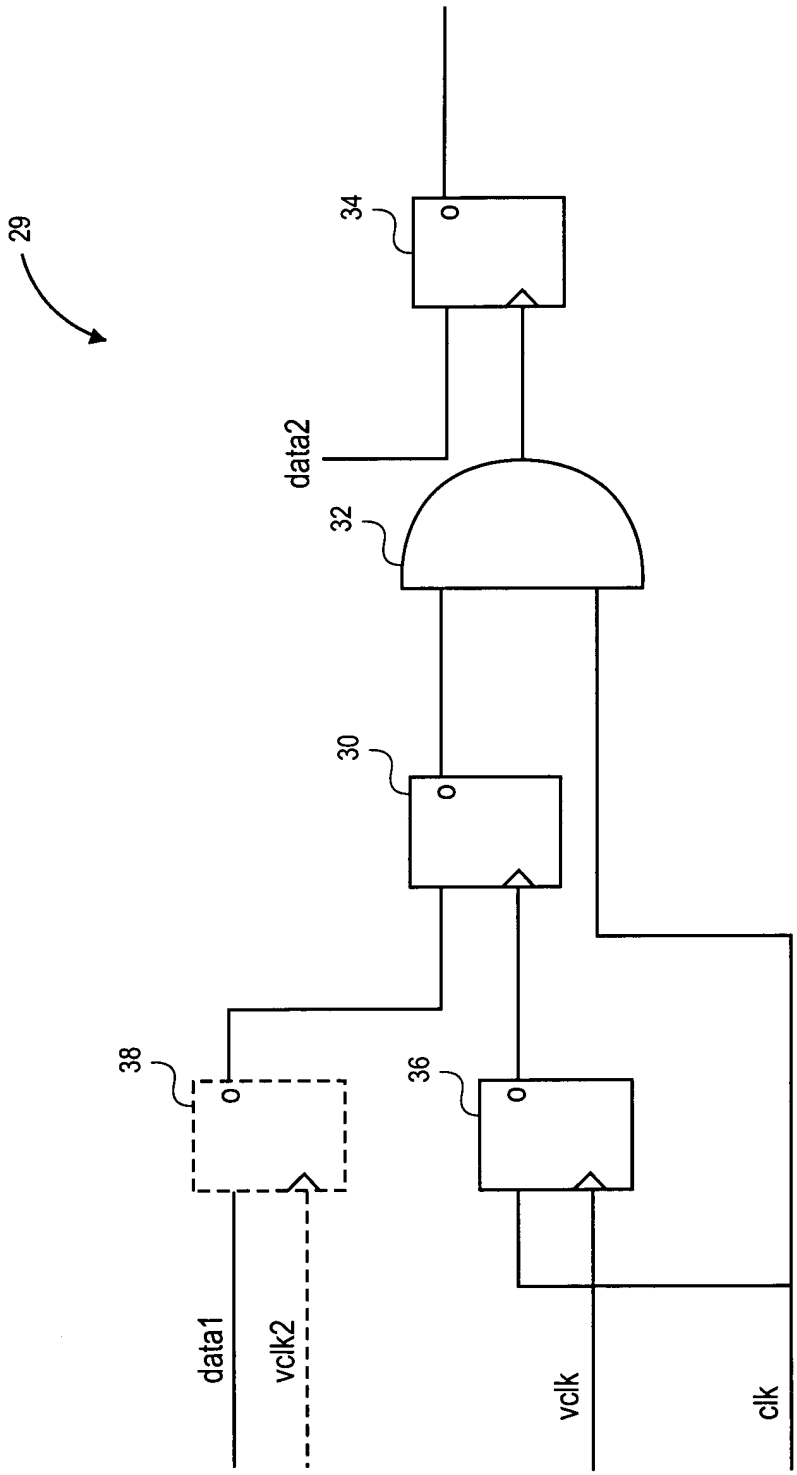

FIG. 4

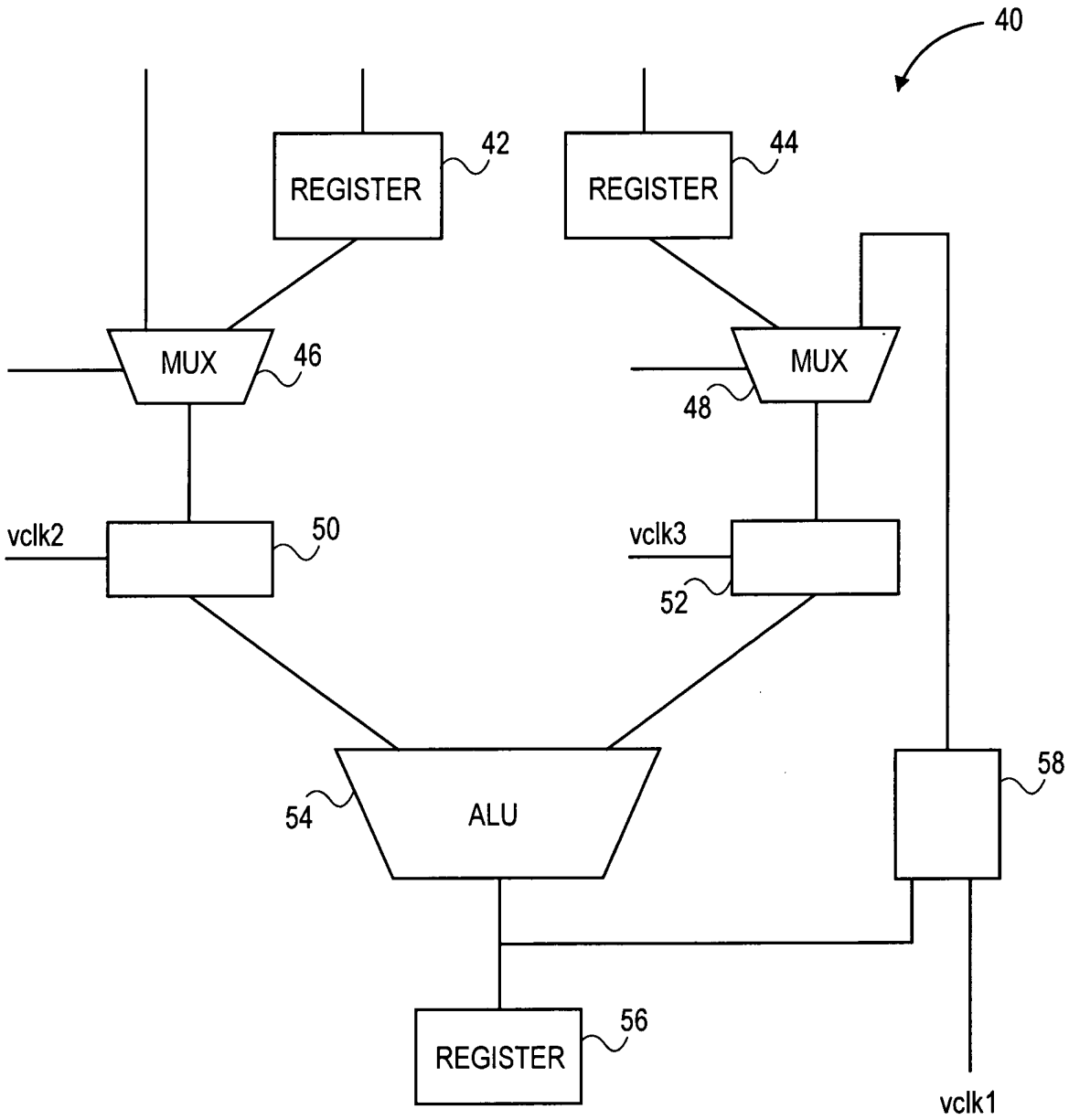

FIG. 5

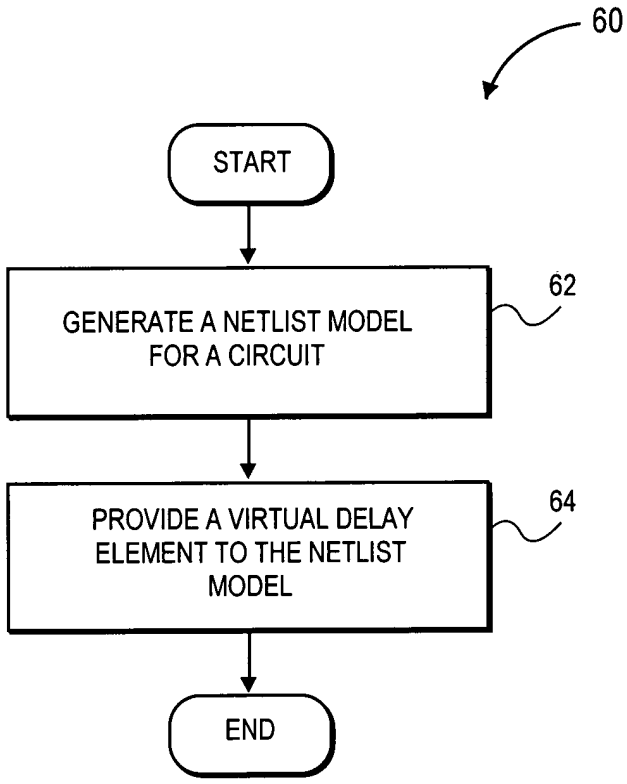

FIG. 6